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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,361	03/12/2004	Masaaki Togashi	119031	5620
25944	7590	10/20/2004	EXAMINER	
OLIFF & BERRIDGE, PLC P.O. BOX 19928 ALEXANDRIA, VA 22320			THOMAS, ERIC W	
			ART UNIT	PAPER NUMBER
			2831	

DATE MAILED: 10/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/798,361	TOGASHI ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Eric W Thomas	2831	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 30 September 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-33 is/are pending in the application.
- 4a) Of the above claim(s) 1-15 and 24-33 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 16-23 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>3/04</u> .  | 6) <input type="checkbox"/> Other: _____                                    |

***Election/Restrictions***

1. Applicant's election with traverse of species B in the reply filed on 9/30/04 is acknowledged. The traversal is on the ground(s) that there is no serious burden on the examiner to examine all the species. This is not found persuasive because the examiner believes there is a serious burden on the examiner (as seen by the distinct species).

The requirement is still deemed proper and is therefore made FINAL.

***Specification***

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

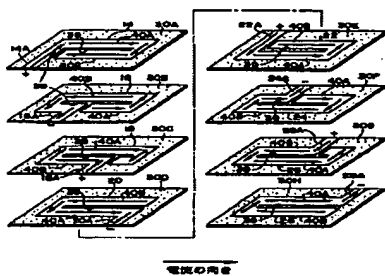
***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 16-17, 22/16-22/17 are rejected under 35 U.S.C. 102(b) as being anticipated by Togashi (JP 2002-164256).



Togashi discloses in fig. 5, a multilayer capacitor comprising: dielectric layers (30A-30H) and at least eight types of first to eighth (40A-40B), internal conductor layers insulated from one another by said dielectric layer and arranged in an order from the first to eighth ones in a dielectric body; wherein each of said first to eighth internal conductor layers is formed with at least one cut part (39); each of said internal conductor layers is formed with a channel part for a current to flow in return by said cut part; and the channel parts in said internal conductor layers adjoining each other across said dielectric layer in the stacking direction carry current flowing in the reverse directions from each other.

Regarding claim 17, Togashi discloses in fig. 5, plane shapes of said first internal conductor layer and said fifth internal conductor layer are symmetric each other with respect to the center of them; plane shapes of said second internal conductor layer and said sixth internal conductor layer are symmetric with each other with respect to the center of them; plane shapes of said third internal conductor layer and said seventh internal conductor layer are symmetric each other with respect to the center of them; and plane shapes of said fourth internal conductor layer and said eighth internal conductor layer are symmetric each other with respect to the center of them.

Regarding claim 22/16, Togashi discloses in fig. 5, a plane shape of the cut part is a substantial linear shape.

Regarding claim 22/17, Togashi discloses in fig. 5, a plane shape of the cut part is a substantial linear shape.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 18-20, 21/16, 21/17, 21/18, 21/19, 21/20, 22/18, 22/19, 22/20, 23/22/16, 23/22/17, 23/22/18, 23/22/19, and 23/22/20, are rejected under 35 U.S.C. 103(a) as being unpatentable over Togashi (JP 2002-164256).

Regarding claim 18, Togashi discloses in fig. 8-9, the first internal conductor layer has a first lead part led to the first side surface of the dielectric body; the second internal conductor layer has a second lead part led to the first side surface of the dielectric body; the second internal conductor layer has a second lead part led to a different position from the first lead part on the first side surface of the dielectric body; the third internal conductor layer has a third lead part led to the second side surface being different from the first and third side surface of the dielectric body; the fourth internal conductor layer has a fourth lead part led to a different position from the third lead part on the second side surface of the dielectric body.

The embodiment (fig. 8-9) of Togashi discloses the claimed invention except for said fifth internal conductor layer has a fifth lead part led to the third side surface on the opposite side of the first side surface of said dielectric body; said sixth internal conductor layer has a sixth lead part led to a different position from said fifth lead part on the third side surface of said dielectric body; said seventh internal conductor layer has a seventh lead part led to the fourth side surface on the opposite side of the second side surface of said dielectric body; and said eighth internal conductor layer has a eighth lead part led to a different position from said seventh lead part on the fourth side surface of said dielectric body. It is well known in the capacitor art to stack like groups of electrodes in an alternating fashion in the capacitor art. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the embodiment of figs. 8-9 of Togashi by adding alternating 1<sup>st</sup> and 2<sup>nd</sup> (5<sup>th</sup> and 6<sup>th</sup> after the 3<sup>rd</sup> and 4<sup>th</sup>) electrodes and 3<sup>rd</sup> and 4<sup>th</sup> (7<sup>th</sup> and 8<sup>th</sup> after the 5<sup>th</sup> and 6<sup>th</sup>) electrodes, since adding more electrodes to the capacitor would increase the capacitance, and it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 3 USPQ 8.

\*As modified, Togashi inherently has the additional structure: said fifth internal conductor layer has a fifth lead part led to the third side surface on the opposite side of the first side surface of said dielectric body; said sixth internal conductor layer has a sixth lead part led to a different position from said fifth lead part on the third side surface of said dielectric body; said seventh internal conductor layer has a seventh lead part led to the fourth side surface on the opposite side of the second side surface of said

dielectric body; and said eighth internal conductor layer has a eighth lead part led to a different position from said seventh lead part on the fourth side surface of said dielectric body.

Regarding claim 19, Togashi discloses the claimed invention except for the width of each of the lead parts is  $1/3$  to  $1/4$  of a width of the channel part in each of the internal conductor layers. It would have been an obvious matter of design choice to form the width of each of the lead parts  $1/3$  of a width of the channel part in each of the internal conductor layers, since such a modification would have involved a mere change in the size of a component, a change in size is generally recognized as being within the level of ordinary skill in the art. *In re. Rose*, 105 USPQ 237 (CCPA 1955).

Regarding claim 20, Togashi discloses a first terminal electrode and a second terminal electrode respectively connected to said first lead part and second lead part are attached to the first side surface of said dielectric body; a third terminal electrode and a fourth terminal electrode respectively connected to said third lead part and fourth lead part are attached to the second side surface of said dielectric body; a fifth terminal electrode and a sixth terminal electrode respectively connected to said fifth lead part and sixth lead part are attached to the third side surface of said dielectric body; and a seventh terminal electrode and an eighth terminal electrode respectively connected to said seventh lead part and eighth lead part are attached to the fourth side surface of said dielectric body.

Regarding claims 21/16, 21/17, 21/18, 21/19, 21/20 Togashi discloses the claimed invention except for the first to eight internal conductors layers are stacked in

this order repeatedly for a plurality of times in the stacking direction respectively across the dielectric layers. It would have been obvious to one having ordinary skill in the art at the time the invention was made to repeatedly stack the first to eight internal conductor layers for a plurality of times in the stacking direction, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 3 USPQ 8.

Regarding claim 22/18, Togashi discloses in fig. 5, a plane shape of the cut part is a substantial linear shape.

Regarding claim 22/19, Togashi discloses in fig. 5, a plane shape of the cut part is a substantial linear shape.

Regarding claim 22/20, Togashi discloses in fig. 5, a plane shape of the cut part is a substantial linear shape.

Regarding claims 23/22/16, 23/22/17, 23/22/18, 23/22/19, 23/22/20, Togashi discloses the claimed invention except for a width of the cut part is 1/10 to 1/3 of a width of the internal conductor layer. It would have been an obvious matter of design choice to form the width of the cut part that is 1/10 of a width of the internal conductor layer, since such a modification would have involved a mere change in the size of a component, a change in size is generally recognized as being within the level of ordinary skill in the art. *In re. Rose*, 105 USPQ 237 (CCPA 1955).

### ***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.



2003/0026059 – Discloses a multilayer ceramic electronic device having a low ESL.

2001/0055191 – Discloses a multilayer ceramic capacitor having multiple electrode leads.

6,441,459 – Discloses a multilayer ceramic capacitor having multiple electrode layers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric W Thomas whose telephone number is 571-272-1985. The examiner can normally be reached on M,Tu,Sat 9 am - 9:30 pm; W, Th, F 6 pm -10:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, consisting of a large, stylized 'E' followed by a 'W' and a 'T'.

Eric W Thomas  
Examiner  
Art Unit 2831

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